Analog Test Bus Enhances Mixed-Signal Debug and Characterization

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In today's complex Mixed-Signal and SOC designs, there is a high demand to provide enhanced test capability while using limited pin resources. Testing the various Intellectual Property (IP) blocks has become an important task in verifying that the block is functionally sound and performing to design specifications. Unlike digital ASIC, microprocessor, or memory devices, which follow more or less standardized DFT processes, each mixed-signal chip or IP design is unique, and presents different debug and characterization needs.

An analog test bus (ATB), has become an important tool in the characterization and debug of analog and mixed signal designs. This type of ATB should not be confused with IEEE 1149.4 analog boundary scan, which is targeted at board level production test capability for analog pins and external components. There are, of course, opportunities to incorporate this type of ATB capability into an 1149.4 design.

In general terms, the test bus is usually a pair of analog lines routed in the design, with analog switches that allow connection to key nodes in the analog circuitry. Two lines are typically used due to the differential nature of many analog circuits. The bus is usually intended for precision DC measurements or in some cases AC measurements where the additional loading will not impact performance. The nodes connected are controlled by a hardware register, which may provide direct parallel access or serial control if the design is pin limited. Some of the nodes typically connected are:

- Ground/Power rails (at various points, to check I/R drop)
- Bandgap references and other internal bias generators
- ADC sample/hold output stages and subrange output stages
- PLL outputs

Shown below is a simplified overview of a typical ATB implementation.

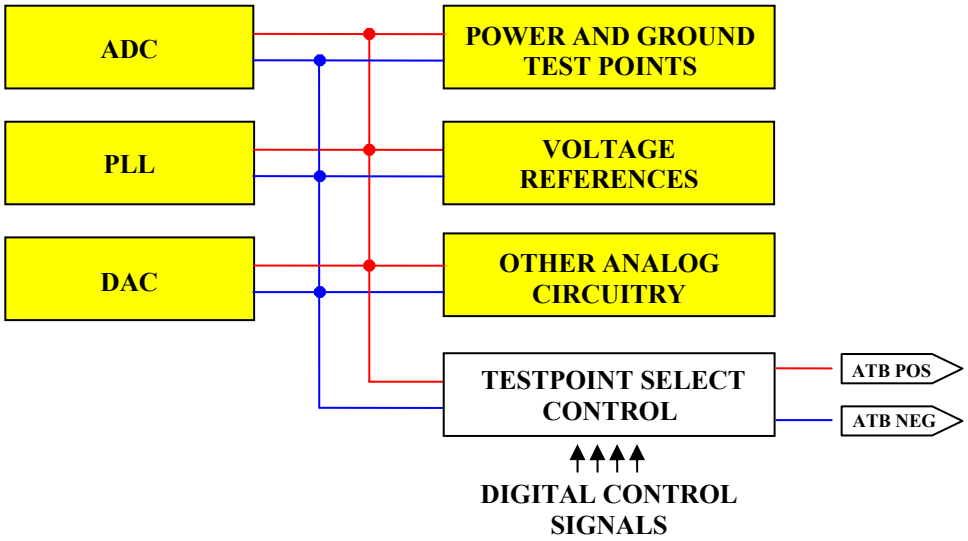

Figure 1

The purpose of this type of test bus is to provide a simple, robust method to access key internal analog nodes of the device. Its value is primarily for improved efficiency during debug and characterization, where verifying specific DC measurements such as bandgap reference voltages and bias currents are crucial in determining the well-being of the device. Without these access points, measurements may be impossible if they have to be taken through other circuitry, or expensive and time consuming if they are taken using methods such as FIB experiments.

As an example, assume a pipelined ADC block in a test chip has an excessive offset error. There are multiple locations in the block where the error could be introduced, such as the sample/hold buffer, or sub-range amplifiers. With an ATB, DC measurements at each stage can be quickly taken to determine where the error is being introduced. The designer can then focus on that specific area, rather than have to guess at where the error might be and run multiple rechecks and simulations. This type of situation is shown below on a simplified example of such an ADC circuit:

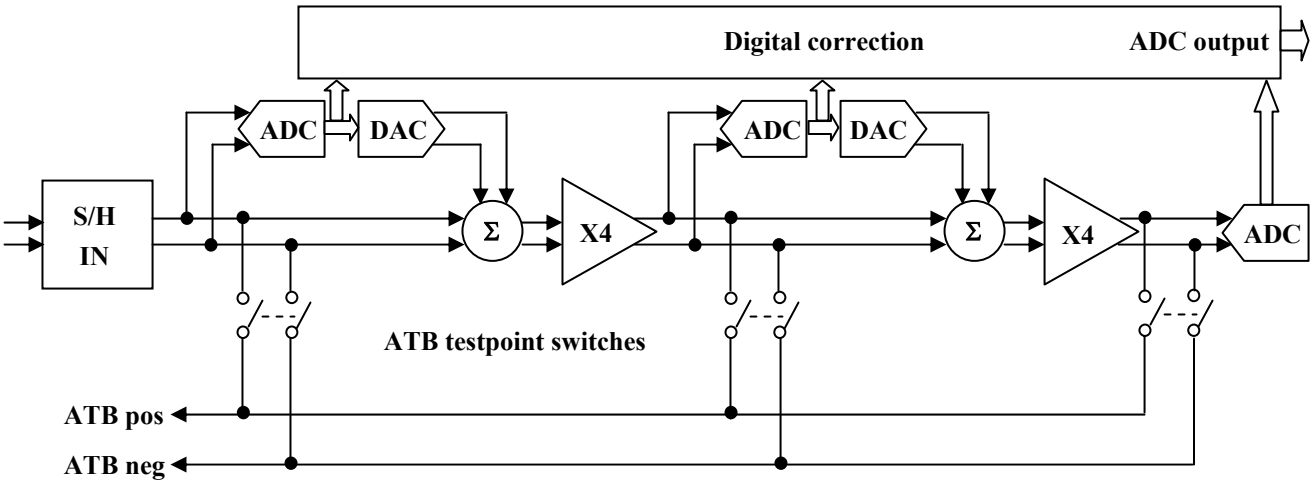

Figure 2

The test bus can also allow overriding an internal voltage or current with an external one, assuming the drive impedance is low enough relative to the circuit node it is driving. This can prove valuable to bypass a section of a design that is not working, allowing other sections to be tested that would not otherwise be possible prior to a re-spin.

As with any built in test scheme, there are performance/test capability tradeoffs that need to be considered. Due to the unique nature of each design, the analog designer or design team is in the best position to analyze these tradeoffs, with feedback and participation from the test engineering group. Some of the considerations are:

- Will adding the analog switches impact mission-mode performance too severely?
- Insure that the test bus drive and bandwidth are appropriate for the type of signals that need to be observed, considering the loading impact of a typical ATE pin
- Impact on noise immunity between the different circuit blocks

In the case of a test chip design, the test bus is usually standard, to maximize visibility into any device performance issues and allow debug. In the case of an actual product, the test bus structures may be connected as a metal mask option, to be included in the pre-production prototypes for initial characterization. Production runs can then be fabricated without the test bus connected, to eliminate any performance issues due to loading.

In conclusion, the ATB provides a useful and simplified method to isolate and test analog circuitry on an SOC design in order to verify functionality and performance. The visibility it provides into the device can provide designers with valuable debug data to compare to simulations. This significantly speeds up the time to market cycle for SOC designs that contain mixed-signal IP.

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